




INRIA has acquired cluster of 104 HP Intel® Itanium™ 2 processor based servers



Created in 1967, INRIA (National Institute for IT and Automation Research) is a public scientific and technological establishment (EPST) that depends on both the Ministry of Research and the Ministry of Economy, Finance and Industry. The principal tasks of INRIA include fundamental and applied research, the design of experimental systems, the organization of international scientific exchanges, the transfer and circulation of knowledge and know-how, and contributions in the field of standards. INRIA employs 1500 scientists, engineers and technicians.

I-Cluster project: high-power computing provided by standard configurations

The ID laboratory (IT and Distribution) was created in 1999. It is an integral part of IMAG (Institute of Applied Mathematics of Grenoble) and carries out research oriented towards concepts, algorithms, tools and software for high-performance, parallel and distributed information systems. Supported by the CNRS, INPG, UJF and INRIA, the laboratory works on four main research themes: parallel programming, clusters and cluster grids, performance and debugging, and the optimization of sequencing. These research themes require an experimental approach and for this purpose, the laboratory manages a "cluster" resource center with its partners.

INRIA Rhône-Alpes launched the I-Cluster project at the end of 2000. Its aim was to respond to the question: "Can computers scattered in a company, or ultimately thousands of machines connected via the Internet, be used as a virtual supercomputer?" In other terms: "Is it possible to use a distributed architecture composed of standard PCs to provide scientists, engineers and more generally industry with the computing power and vast memory space that can compete with dedicated supercomputers?"

HP immediately became involved in the I-Cluster project. HP supplied the ID laboratory with 225 HP eVectra equipped with the Intel® Pentium® III processor 733 MHz with 256 Mb of RAM. These are standard machines that any company can purchase via conventional distribution channels. In parallel, HP laboratories made several system engineers available to INRIA to successfully conduct performance tests. The results are as surprising as they are conclusive and for good reason: the PC cluster was ranked 385th machine in the world among the Top 500 of June 2001. "This was a worldwide first in that the supercomputers in the Top 500 were either proprietary machines, or highly 'supercharged' PCs", states Philippe Augerat who leads a large number of projects in the ID laboratory, in particular those on PC clusters.

Intel® Itanium® 2 for increased power

Whether involving benchmarking, matrix calculations, etc., high-performance applications used by scientists are increasingly voracious users of computing resources, a field traditionally reserved for 64-bit machines. This is why INRIA, acting on behalf of its partners (CNRS, INPG, UJF and ENS of Lyon) and with funds supplied by the MENRT, the Rhône-Alpes regional council, ENS of Lyon and INRIA, launched a call for bids in early 2002 to equip itself with a new PC cluster with even higher performance. Several manufacturers were contacted and it was the HP offer, built around the Intel® Itanium® 2 processor, that was accepted by INRIA. There were several reasons for this, as Philippe Augerat explains: *"The IA64 architecture of the Itanium 2 is in perfect accord with the nature of the scientists' activity, which features predictive and innovative work. In addition, there was a considerable financial attraction, since the HP/Intel Itanium 2 offer was highly competitive."* Its attractiveness to researchers carrying out high-performance computation activities and to all users faced with major memory and flow-rate problems (system and memory buses with IA32 architectures) also contributed substantially to the adoption of the Intel Itanium 2 processor. INRIA also relied on tests carried out by members of the "Observatoire de Grenoble" (Grenoble Techno-Watch) who assessed the performance of the Intel Itanium 2 processor in the field of astrophysics applications. *"Their evaluation was very positive. That was the basis of our decision, since researchers are the reference in the field of computation."*

In October 2002, INRIA ordered 104 HP Itanium 2-based 900 MHz bi-processor nodes, with 3 Gb of RAM. These machines were distributed in 5 racks of 20 nodes, supplemented with four other machines used as an independent server for sequential calculations. Delivery is planned for early 2003, and it will be one of the first IA64 clusters. The HP/Intel Solution Center has been key in the validation of the solution: the porting to Itanium 2 of the Linux-Mandrake distribution as well as the tools co-developed by MandrakeSoft and



Inria within the CLIC research project has been performed there. A privileged and secured access locally and remotely has been provided as well as the technical support needed for the validation. *"We are also working with Intel France on highly technical issues involving the processor itself. We are very lucky to have HP and Intel alongside us"* concludes Philippe Augerat, who hopes to move far up the ladder of the next Top 500 fastest machines in the world. This machine will enable us to implement and benefit from innovative research prototypes supported by research projects in the Rhône-Alpes Region: large-scale memory management, high-performance and high-availability programming environments, virtual-reality and imaging applications, life sciences applications and more. It will be connected to a national grid that should include about 5,000 machines and will be one of the principal nodes open to the entire academic community. The success of this project is due to personnel of HP laboratories, the support of HP Annecy, HP sales teams and Intel technical staff.

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Intel® Itanium® 2

The Itanium® 2 processor builds on and broadens the bases laid down by Intel® Itanium® architecture. It has binary compatibility with its predecessor and provides performance gains of 50 to 100%. It is equipped with considerable execution resources, a main bus with a 6.4 Gb/s bandwidth and a built-in level 3 cache with a capacity of 3 Mb. This means it can achieve, at a lower cost, a transactional efficiency in certain cases 50% above comparable RISC architecture systems.